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FIG. 1

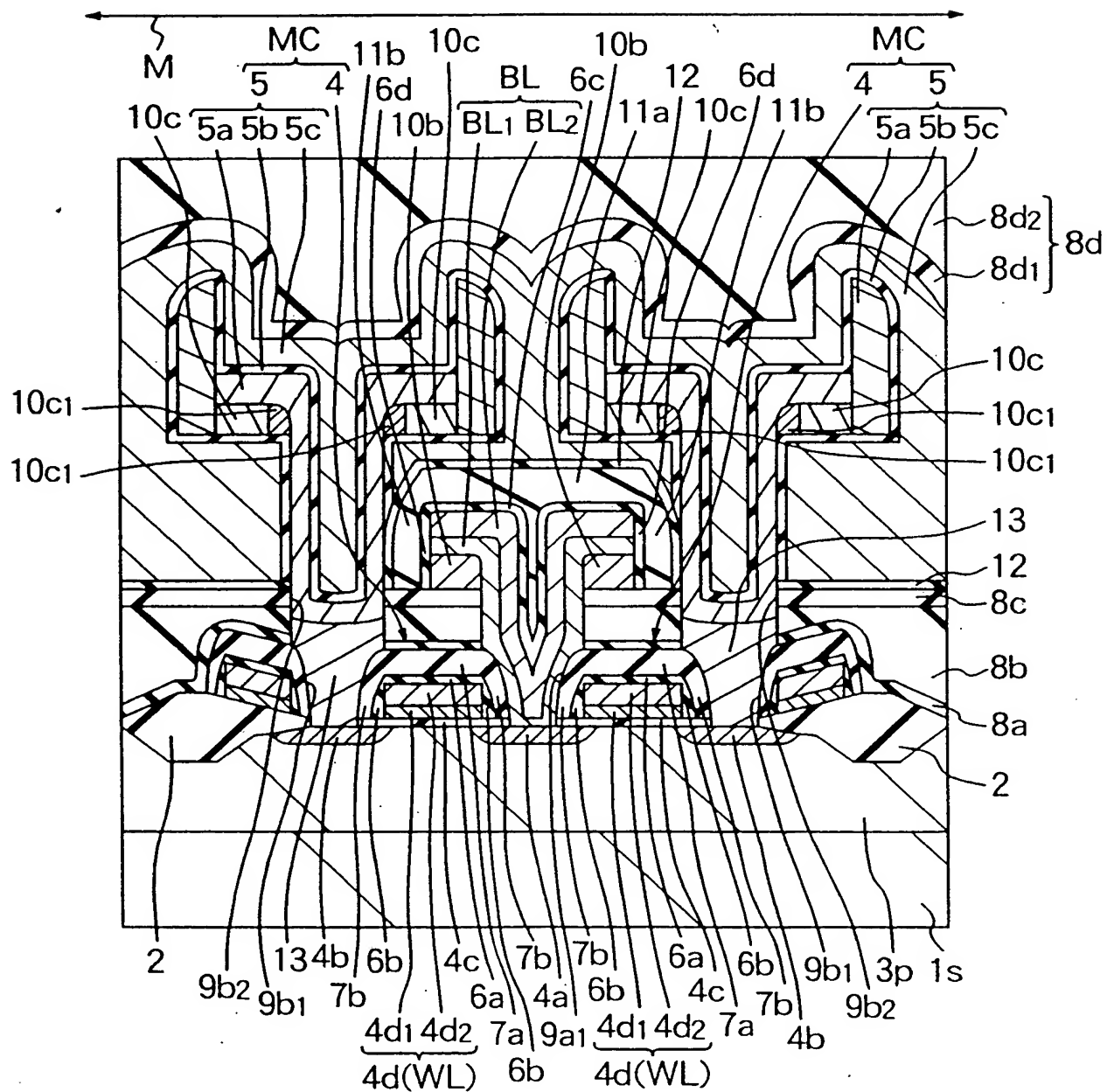


FIG. 2

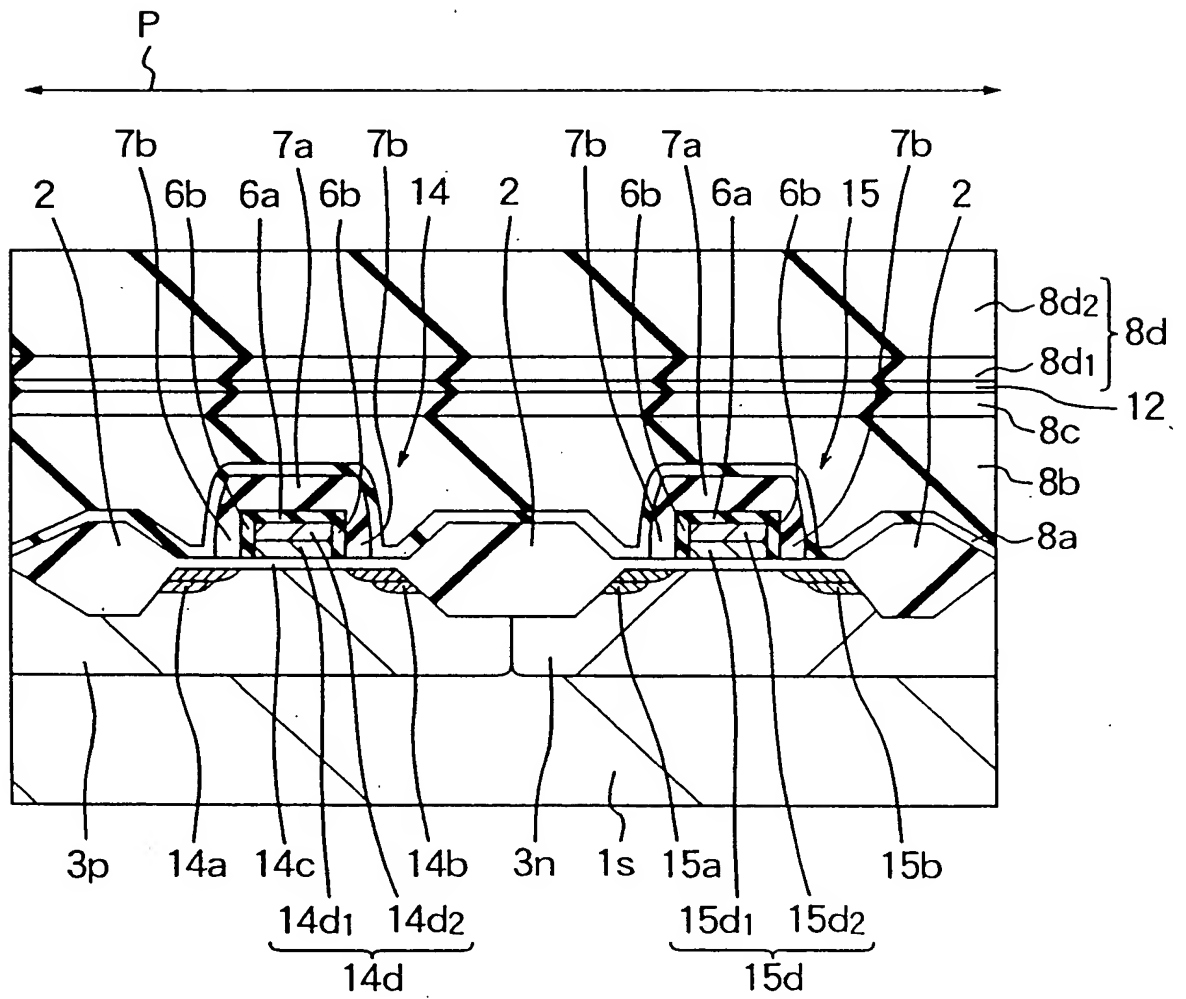


FIG. 3

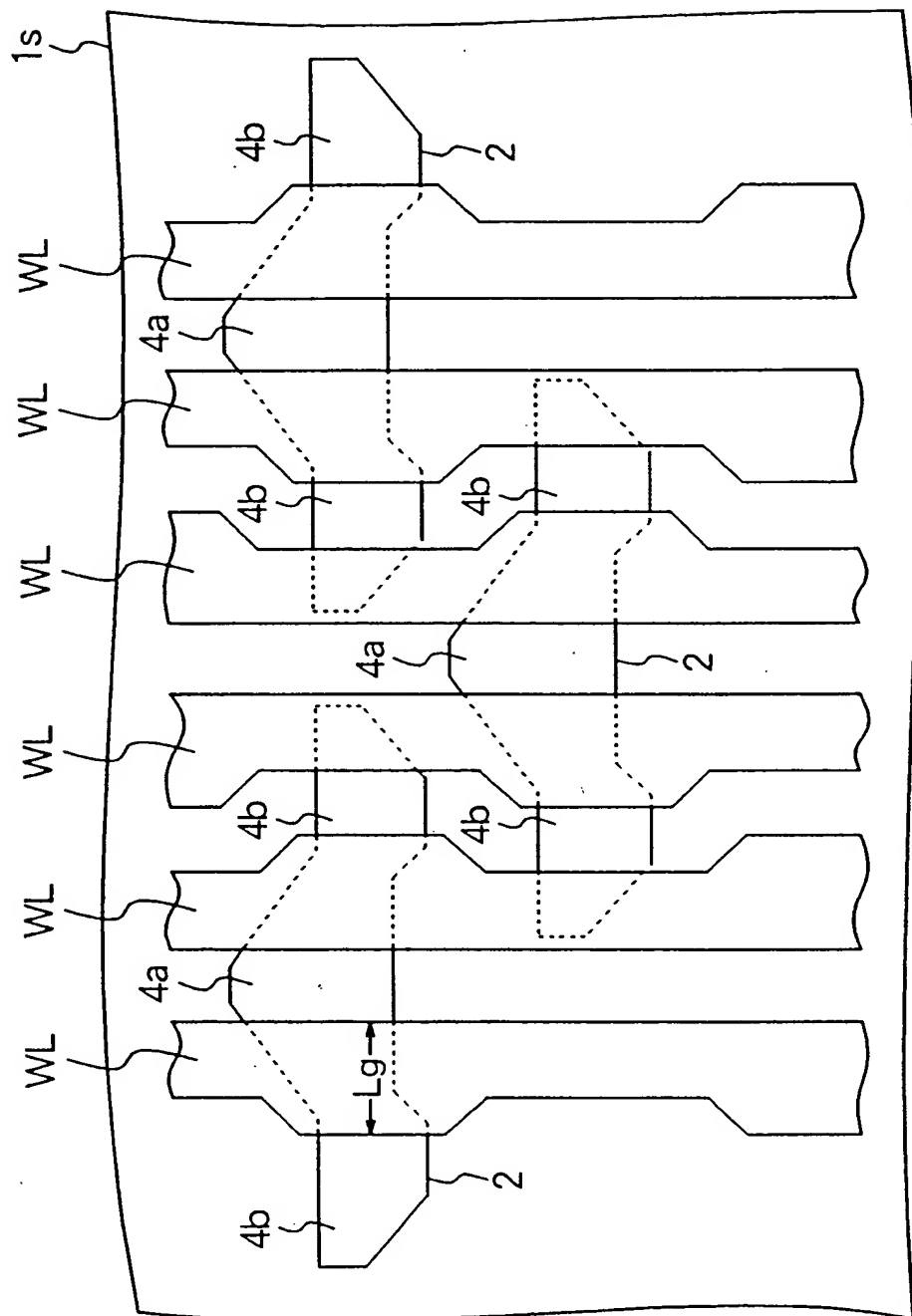


FIG. 4

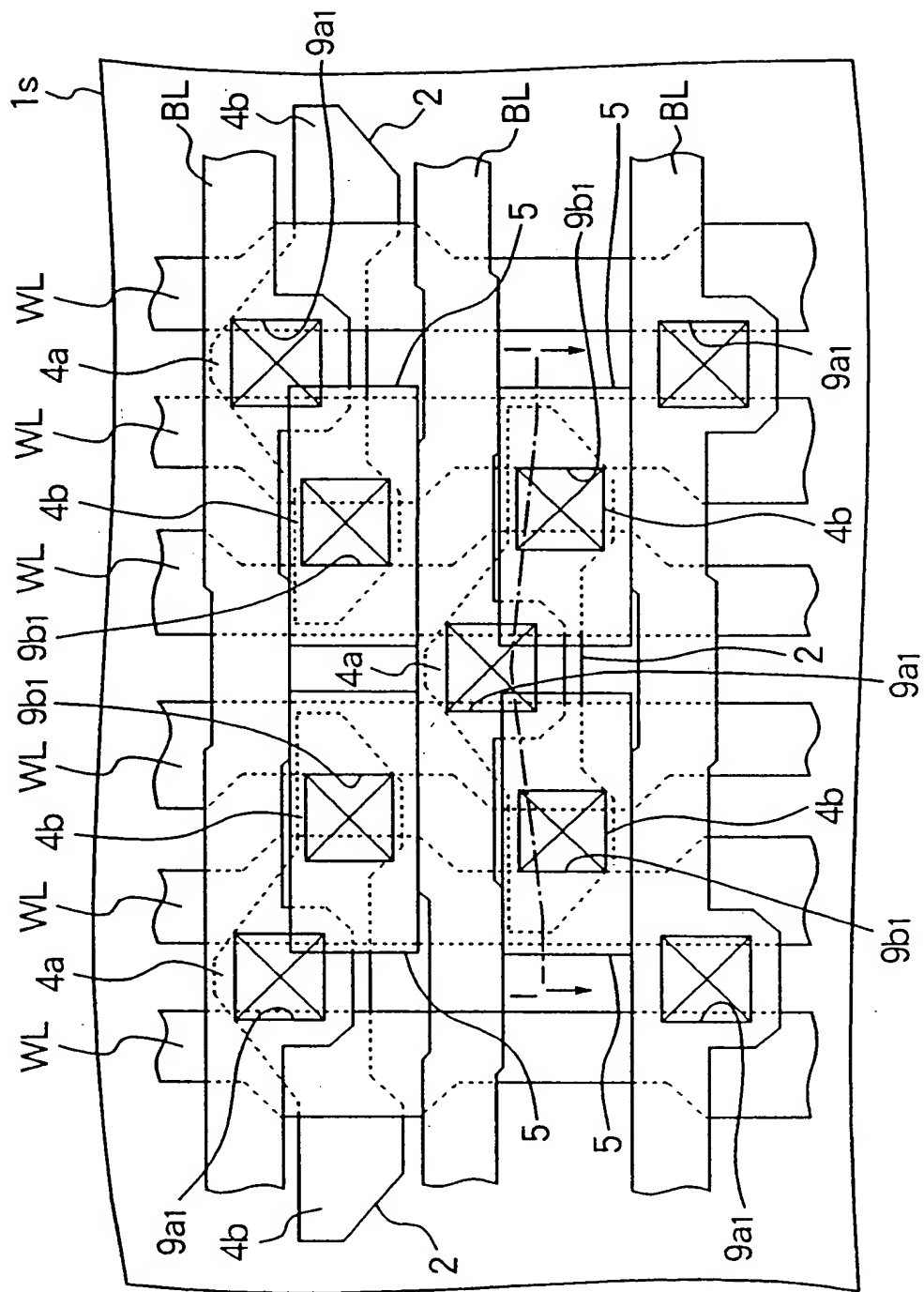


FIG. 5a

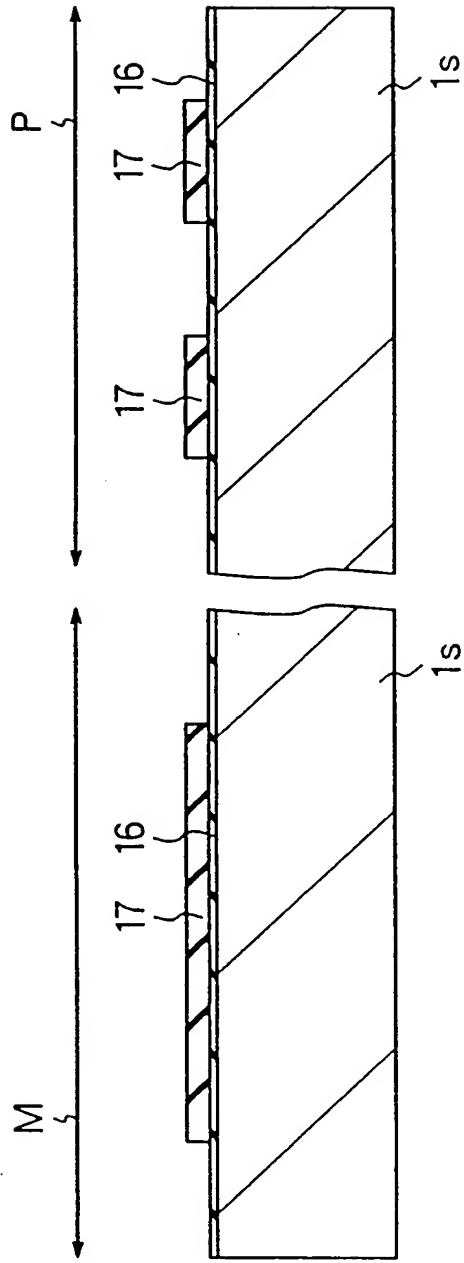


FIG. 5b

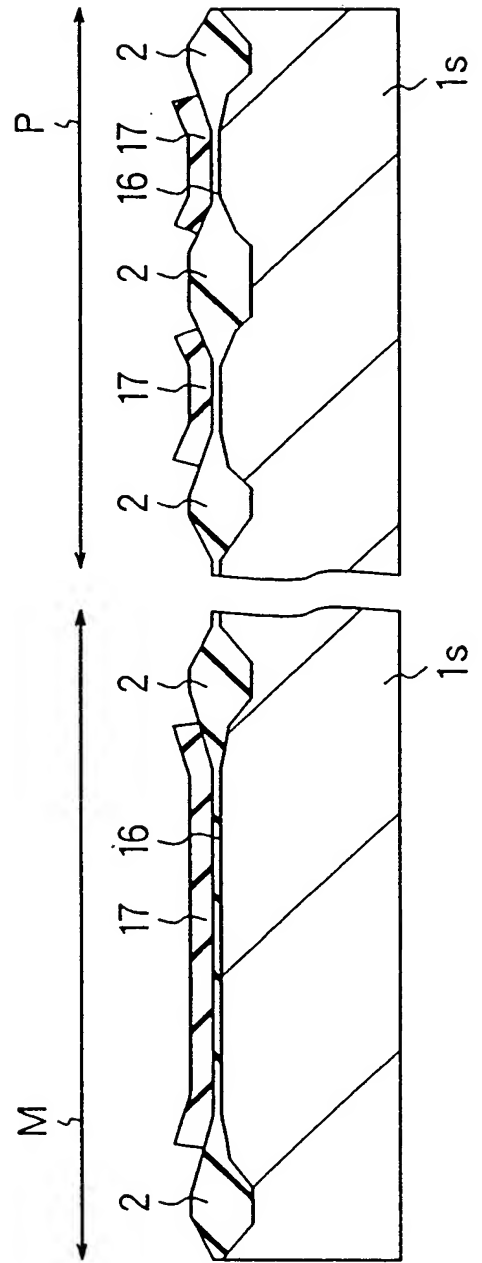


FIG. 5c

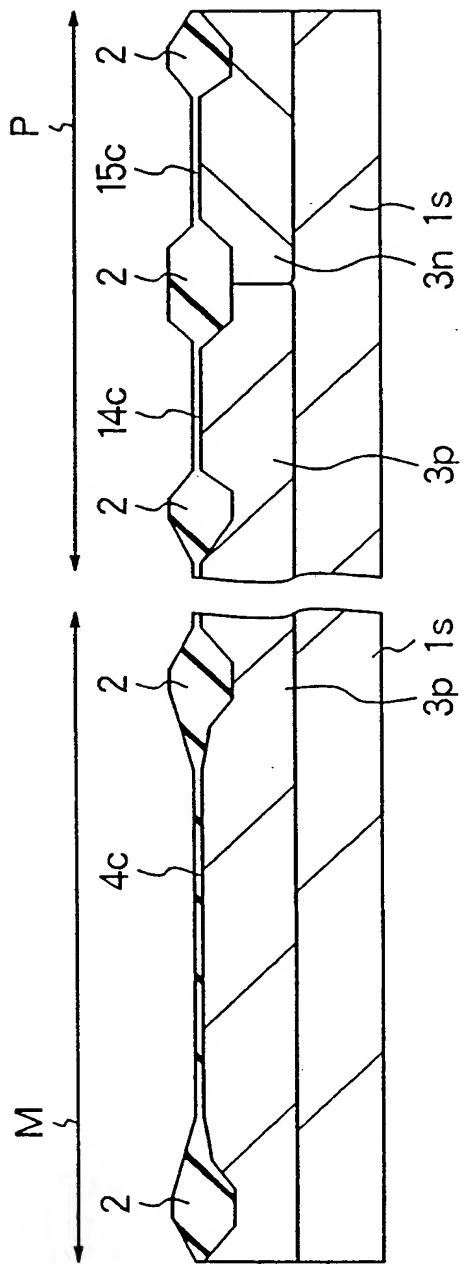


FIG. 5d

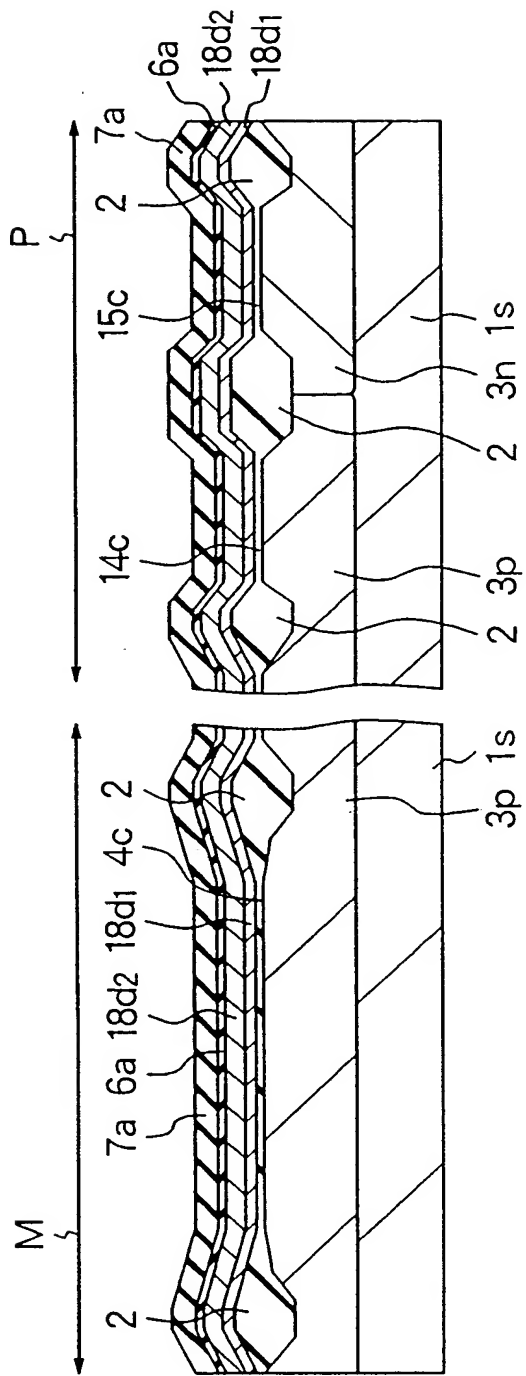


FIG. 5e

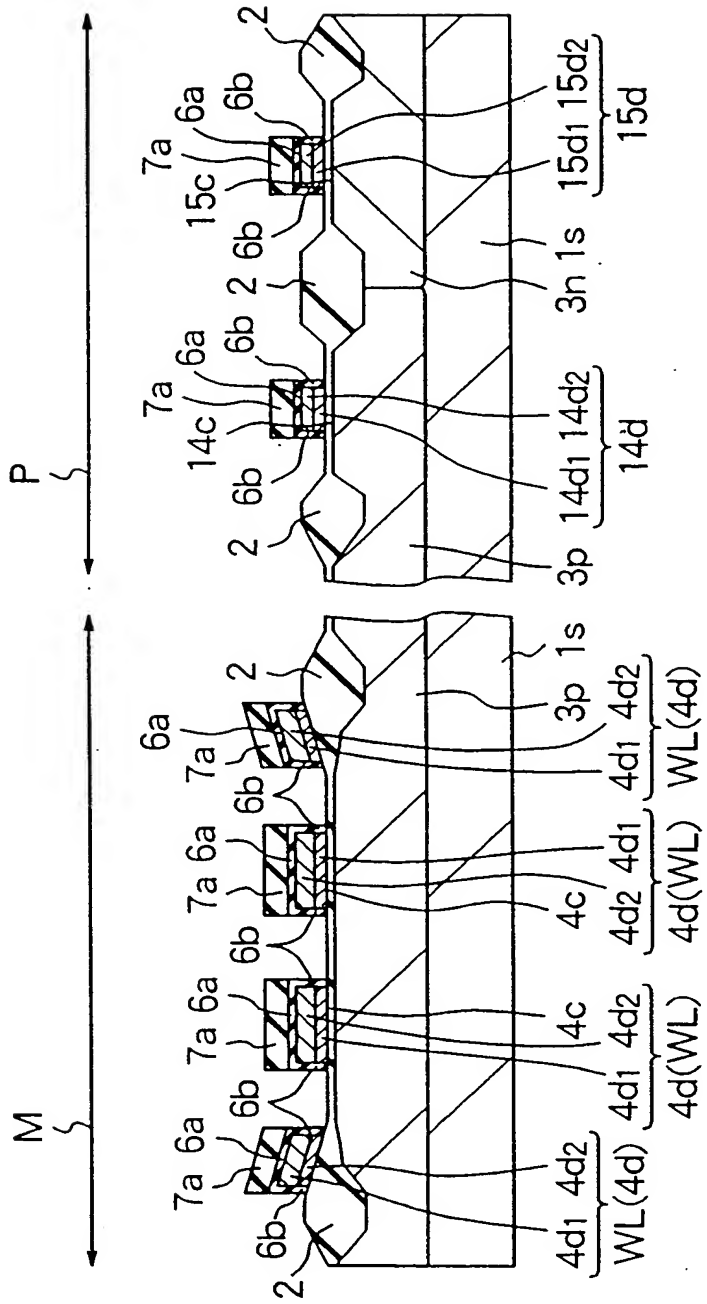




FIG. 5h

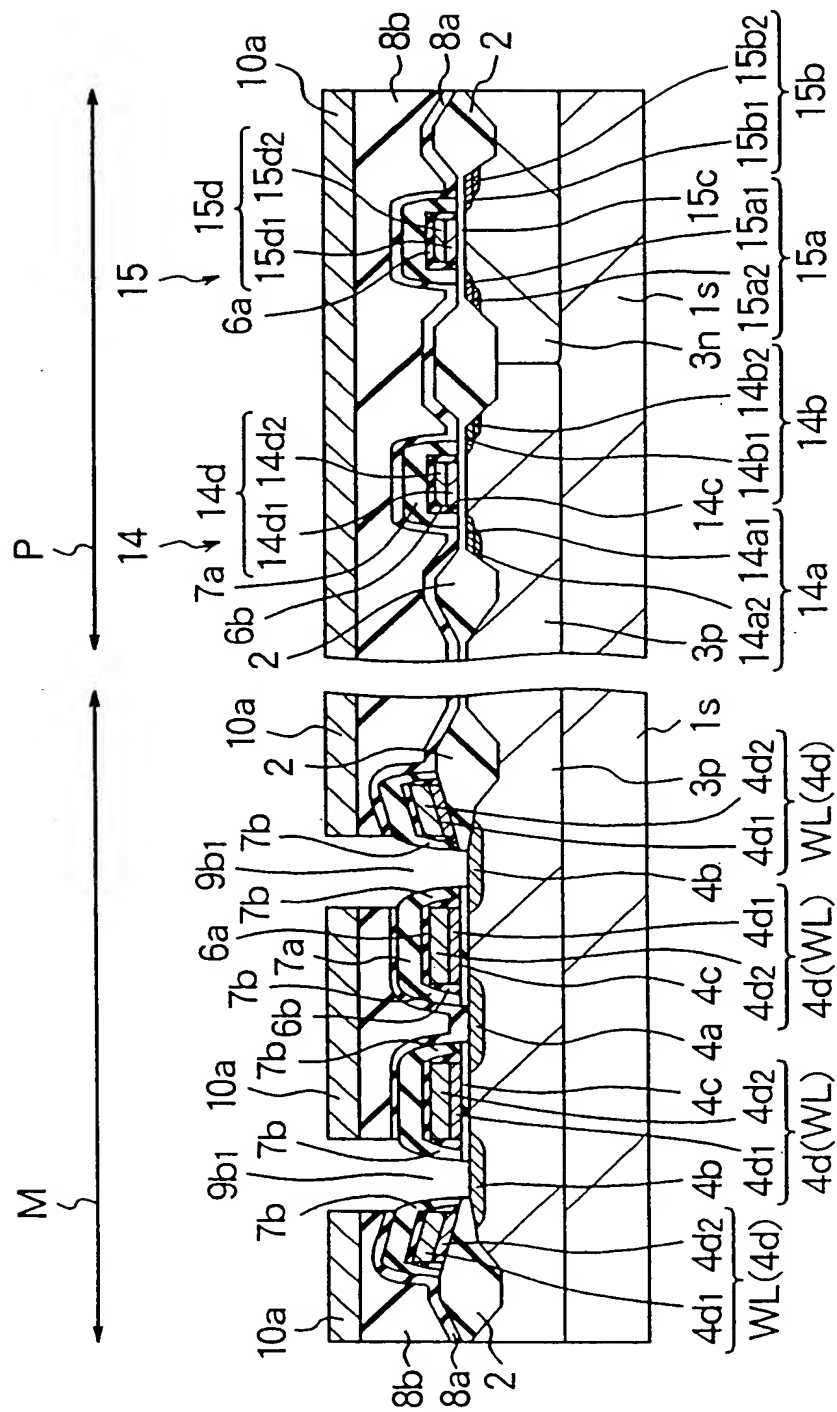


FIG. 5k

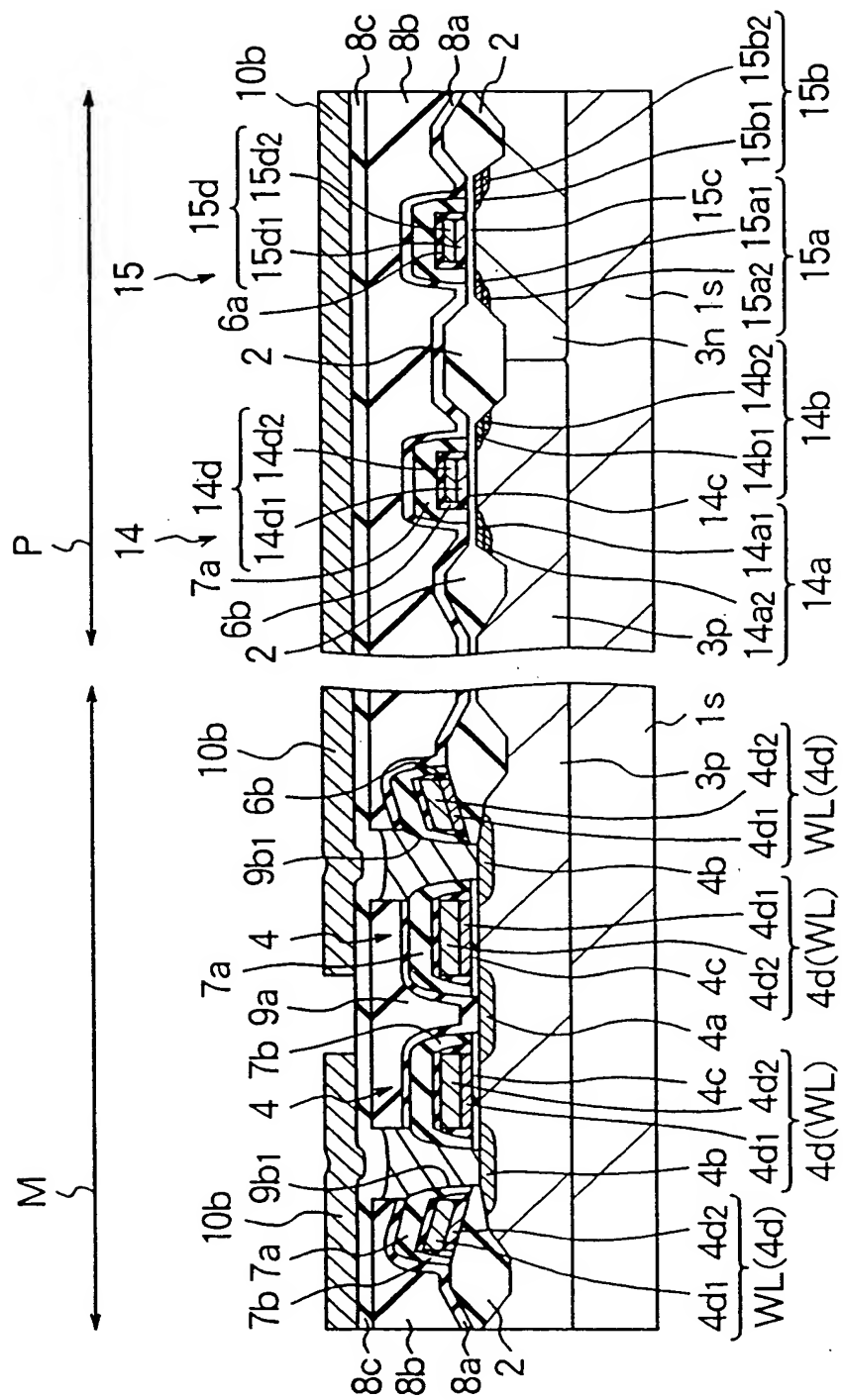


Figure 1 shows two cross-sectional views of a semiconductor device, labeled M and P. The device is shown in a cross-section along a line P-P. The device includes a substrate 2, a gate stack 10b, and various conductive layers and contacts labeled with numbers 1 through 15b. The left view (M) shows a state with a conductive layer 11a and a gate stack 19a. The right view (P) shows a state with a conductive layer 11a and a gate stack 19a. The device includes a substrate 2, a gate stack 10b, and various conductive layers and contacts labeled with numbers 1 through 15b.

FIG. 5n

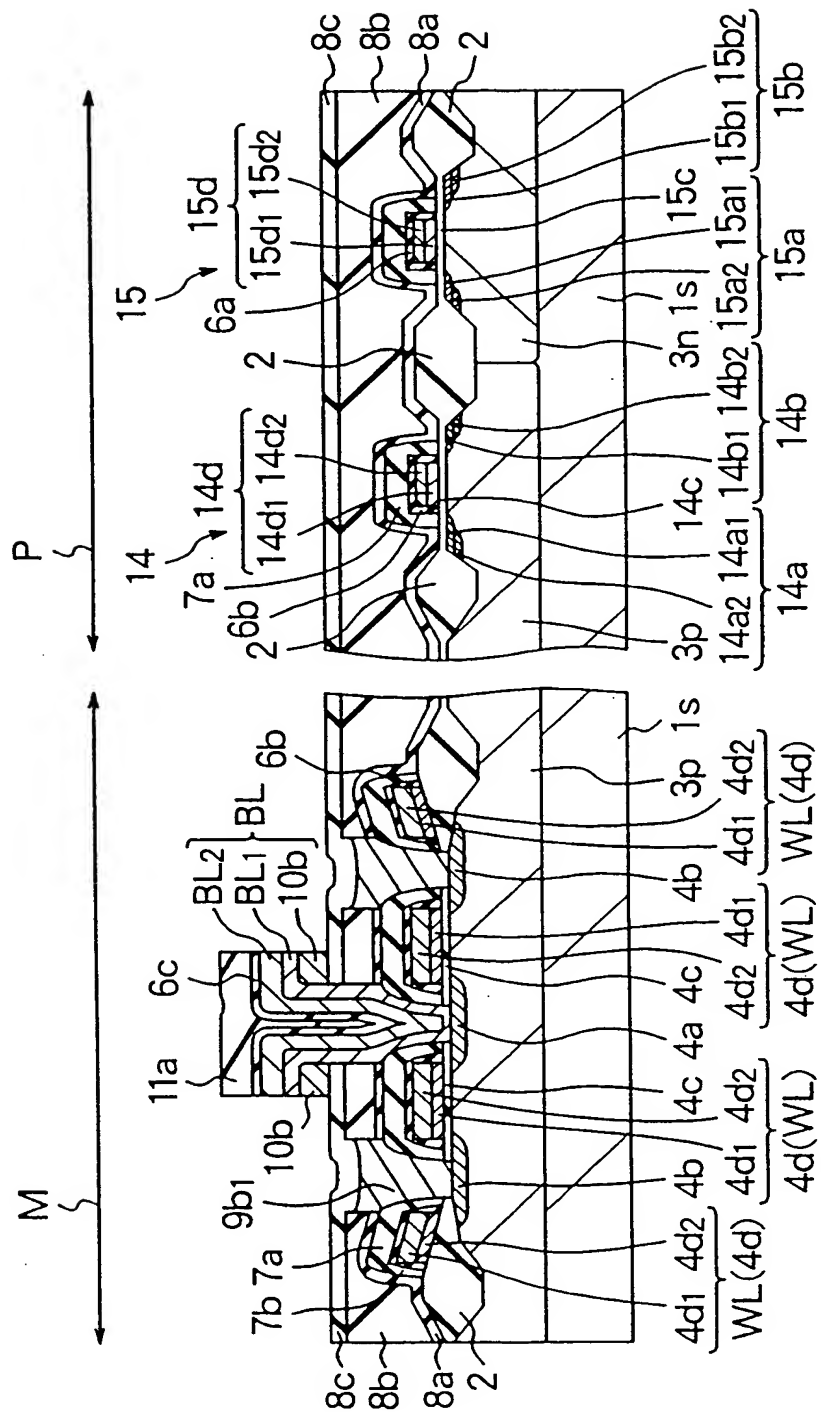


FIG. 50

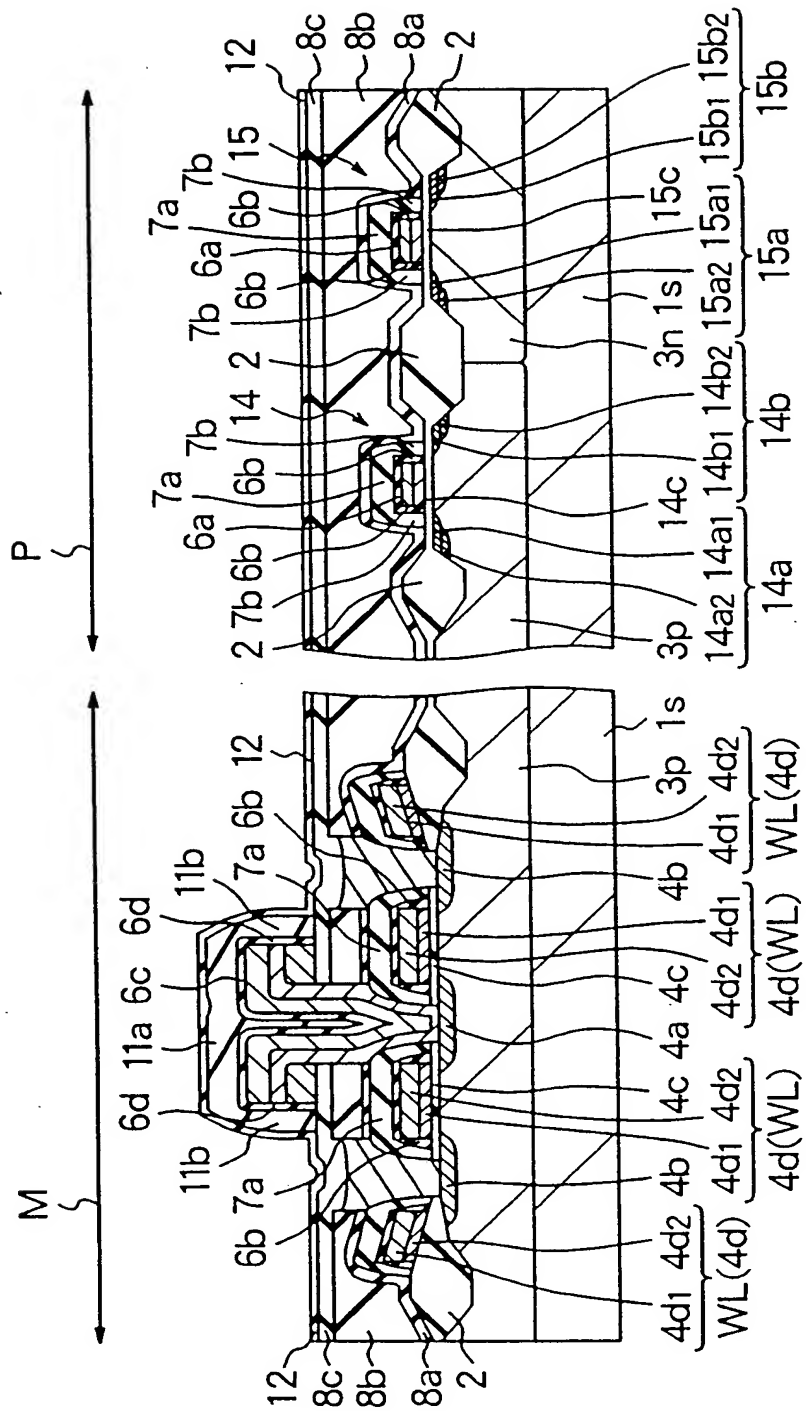


FIG. 5p

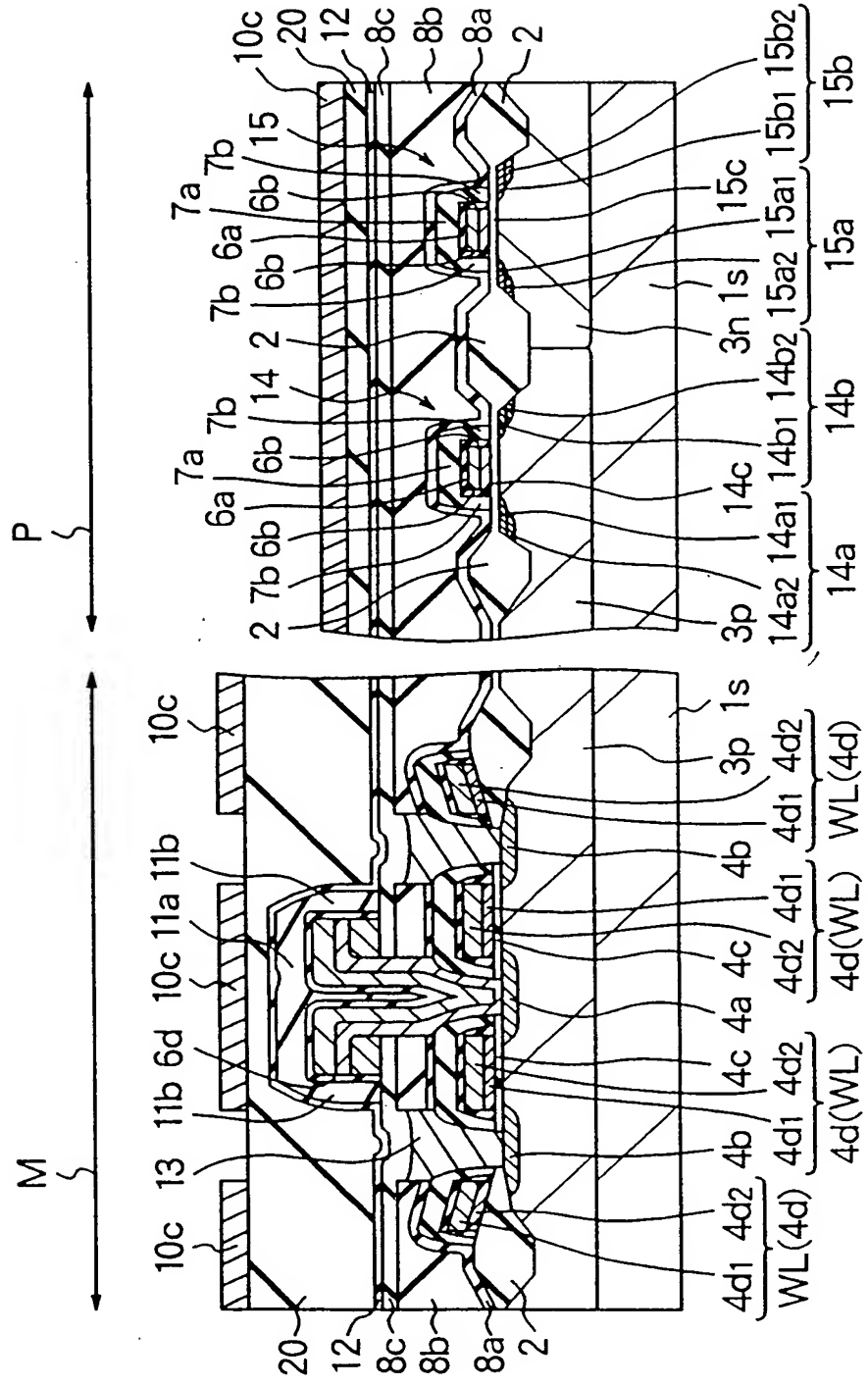


FIG. 5q

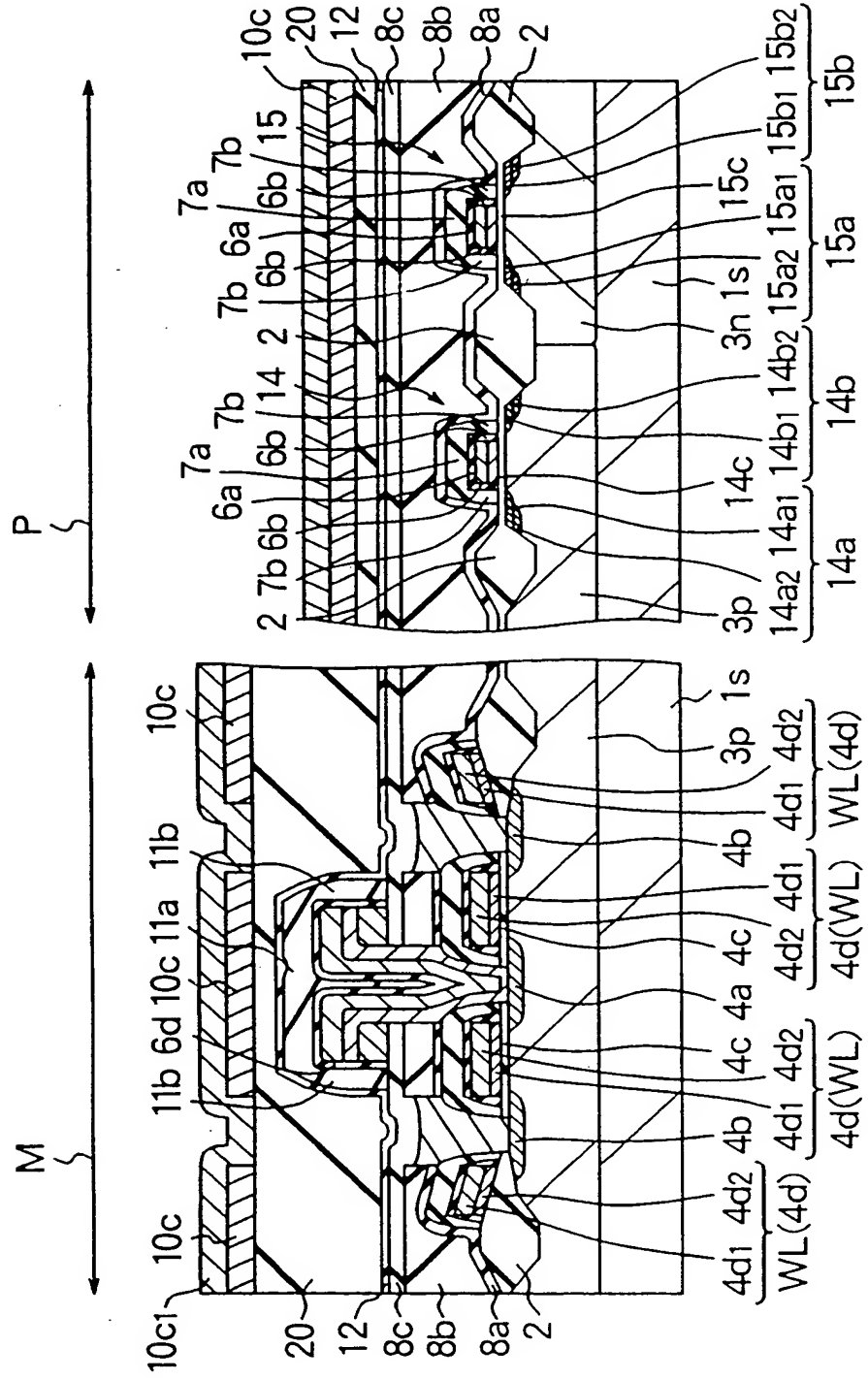
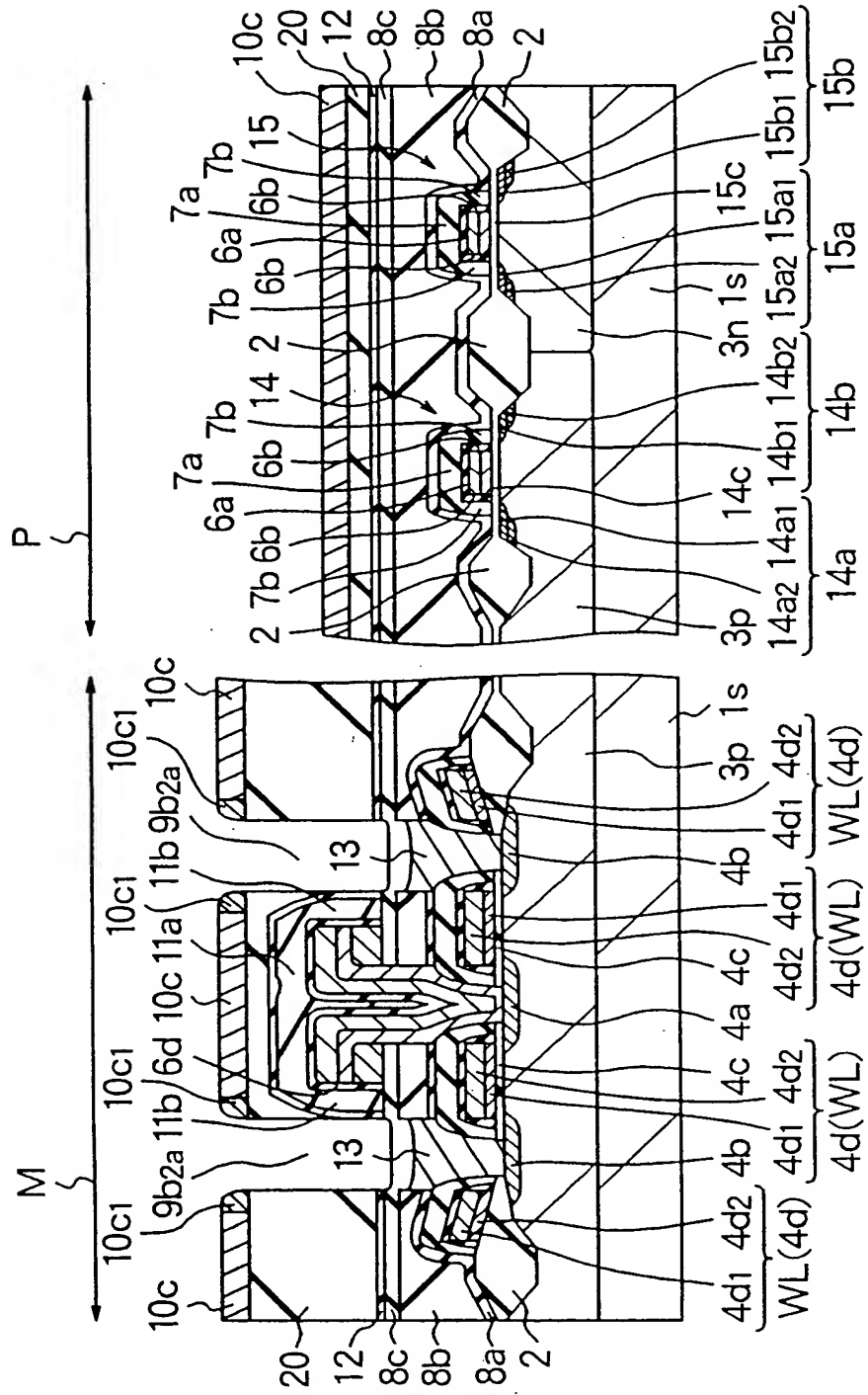


FIG. 5s



[illegible]

FIG. 5u1

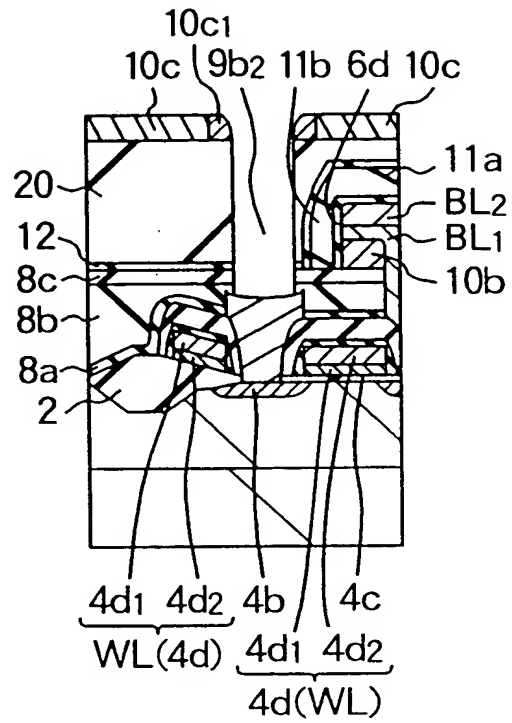


FIG. 5u2

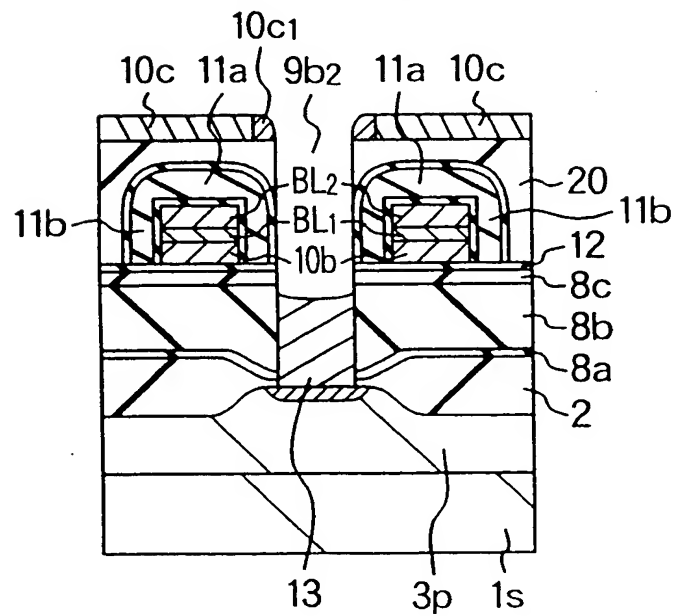
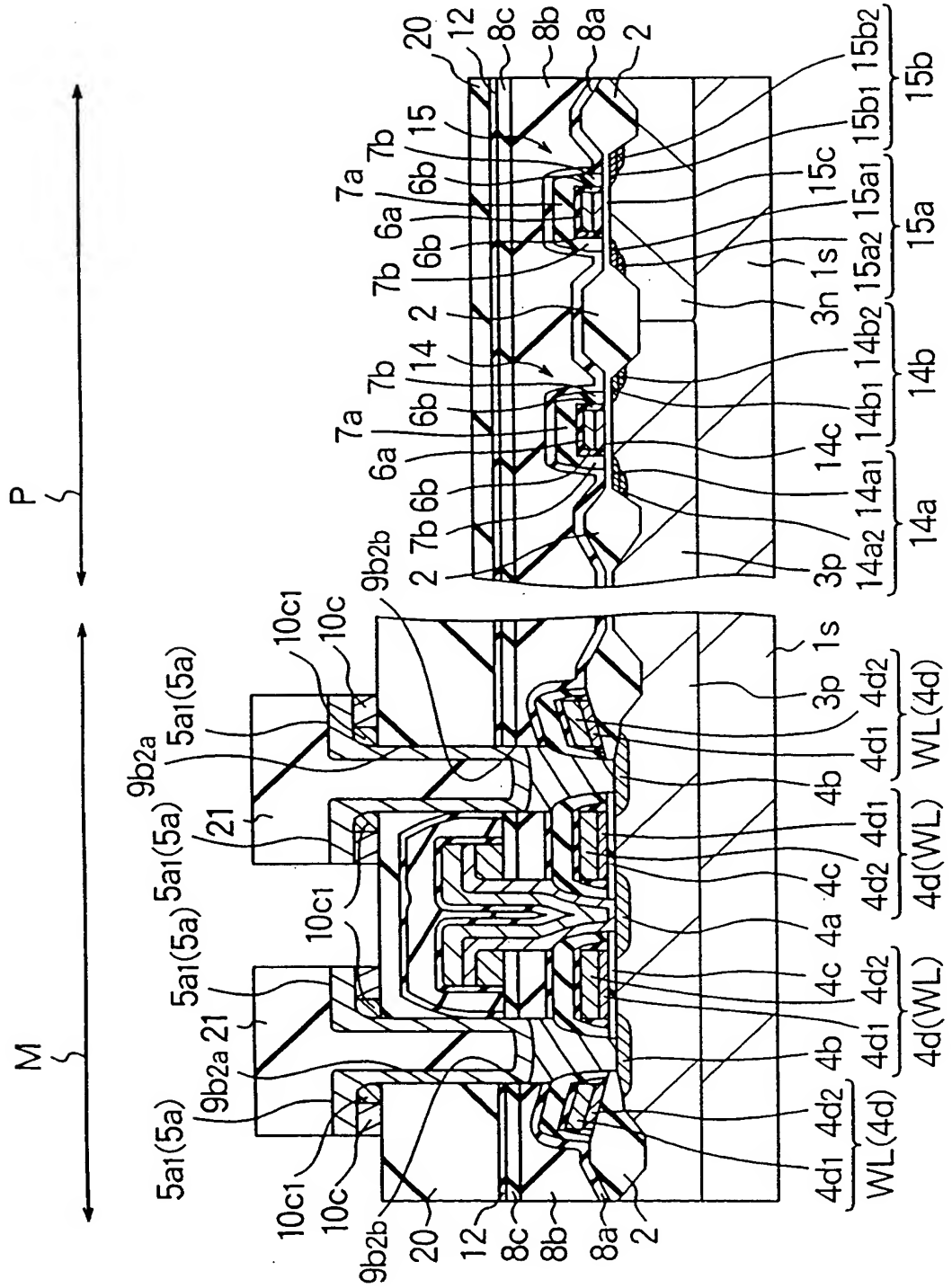


FIG. 5v



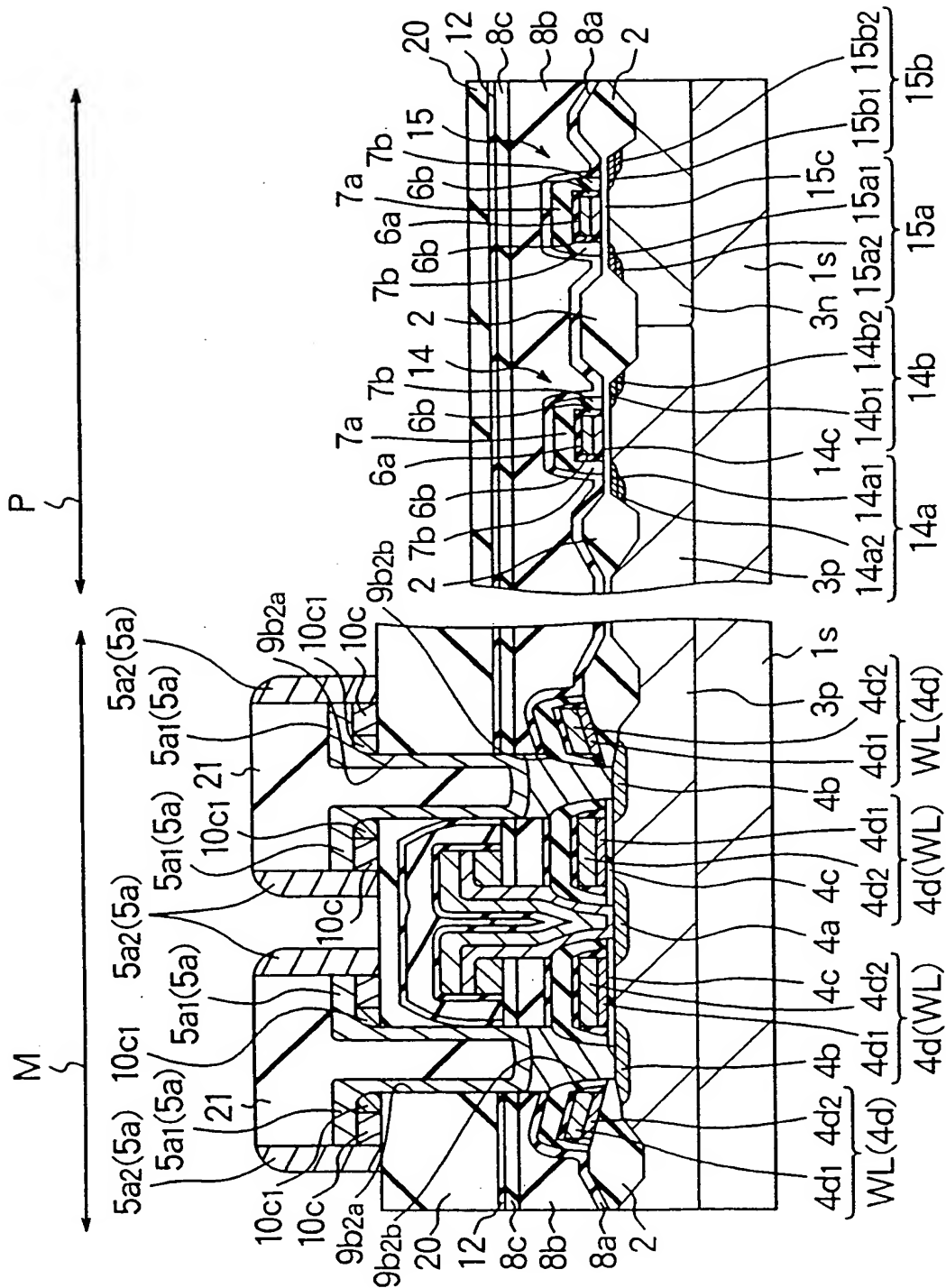


FIG. 6a

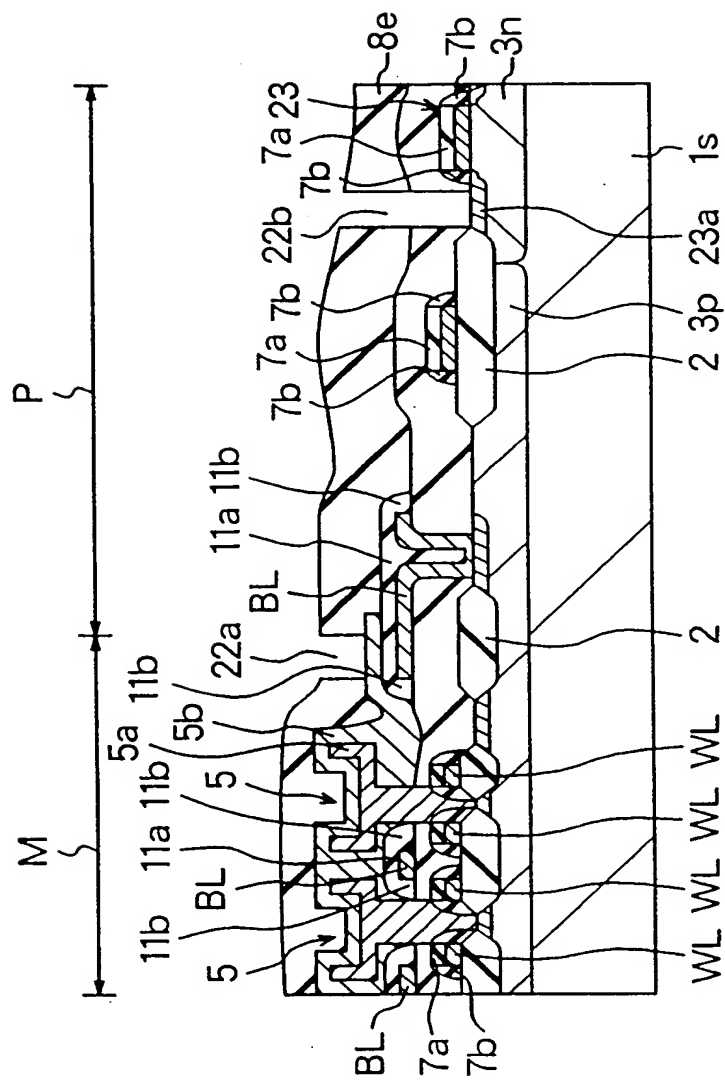


FIG. 6b

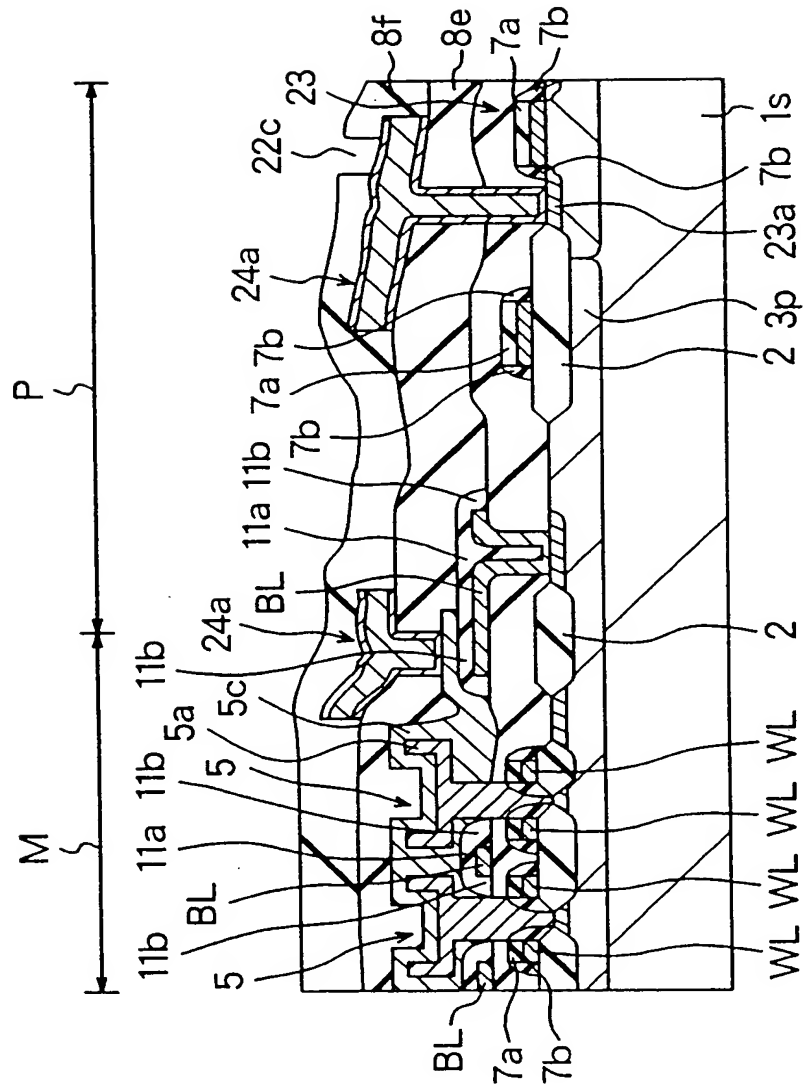


FIG. 6c

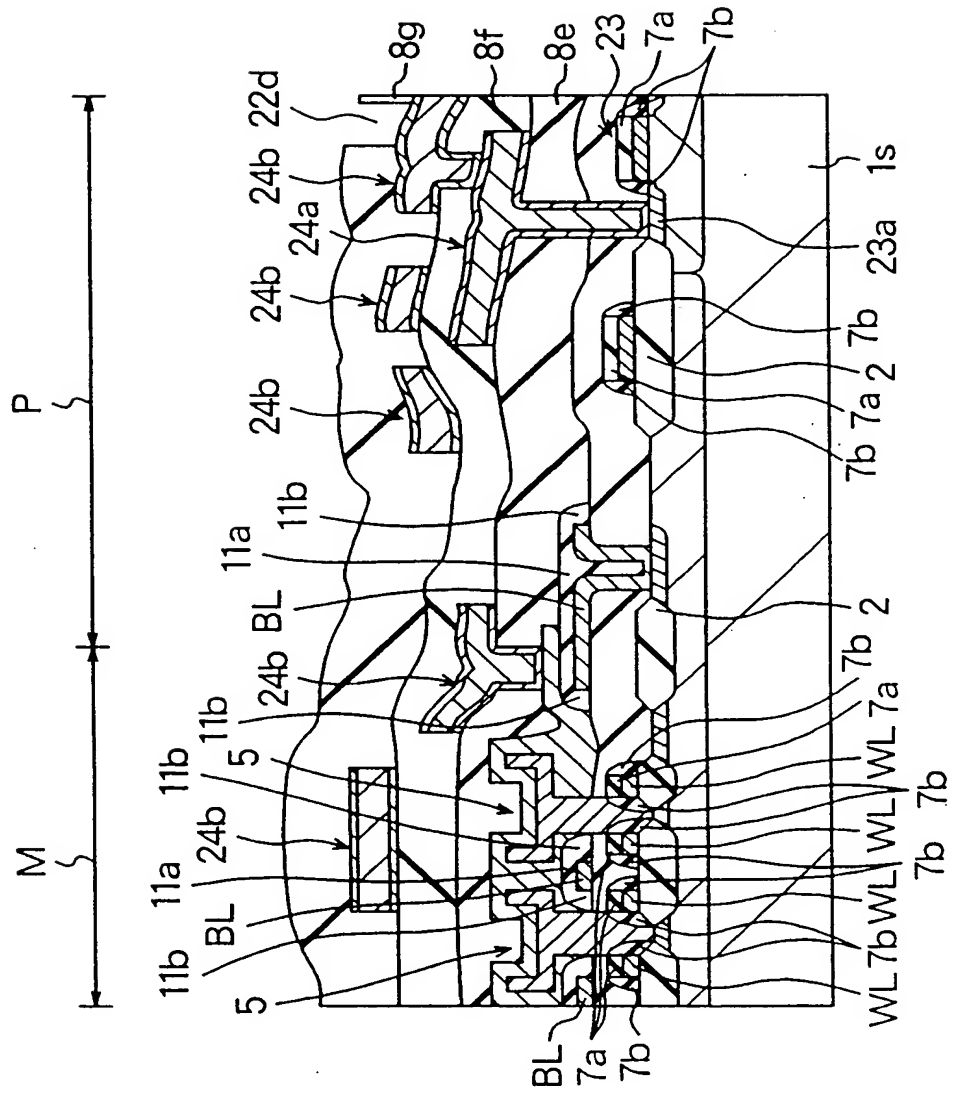


FIG. 6d

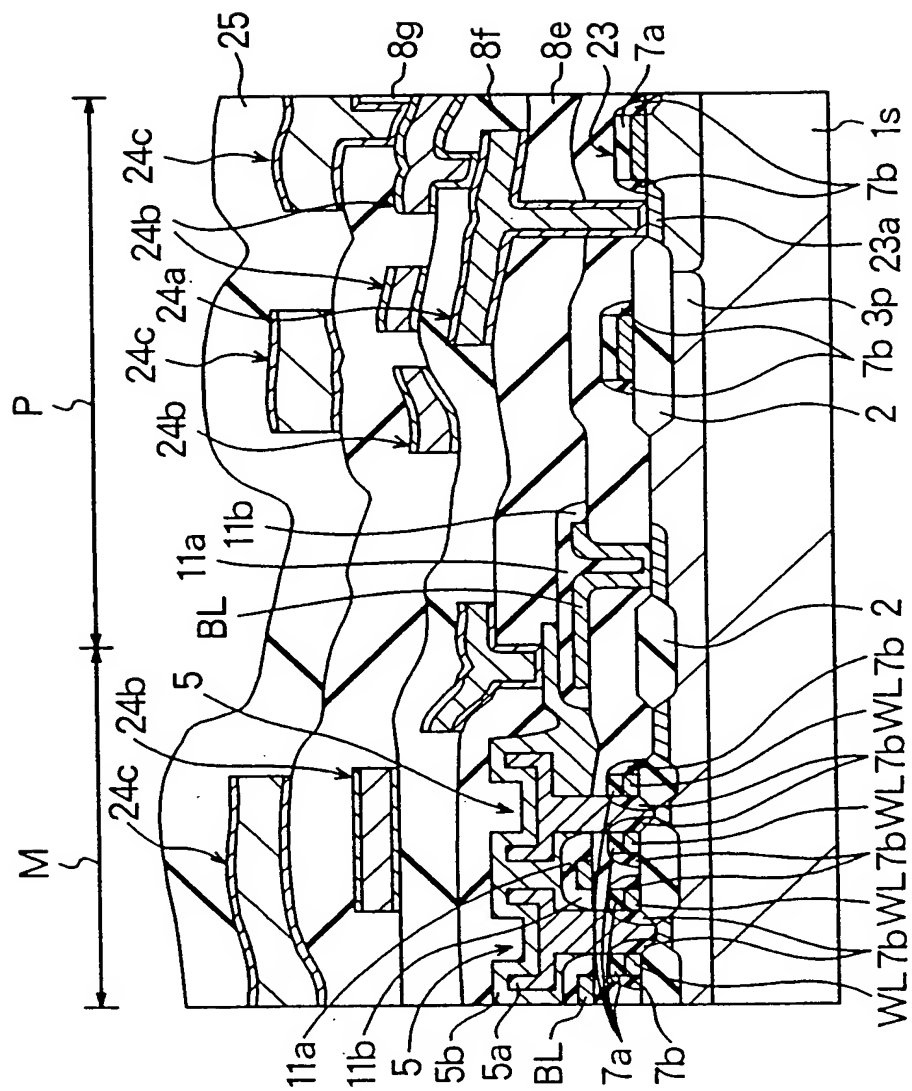
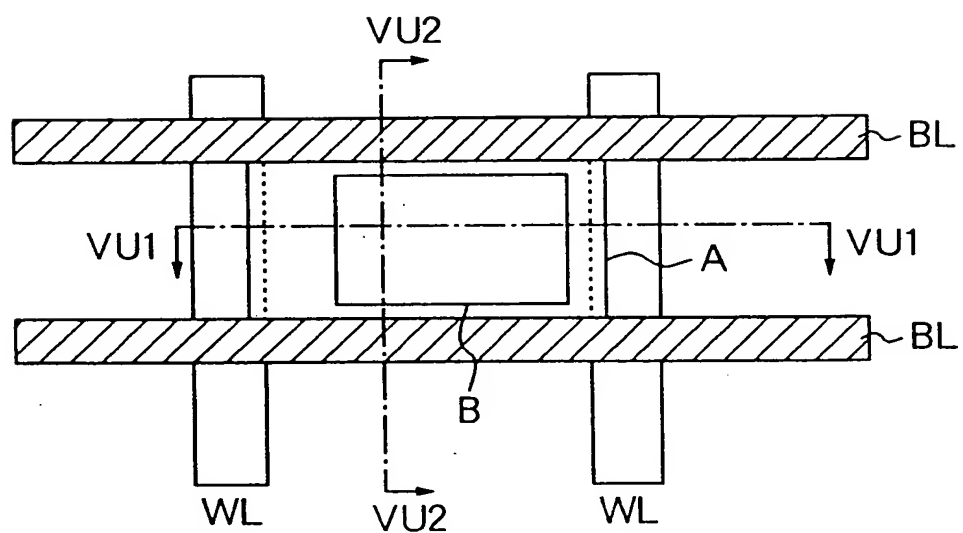


FIG. 7



[illegible]

FIG. 9a

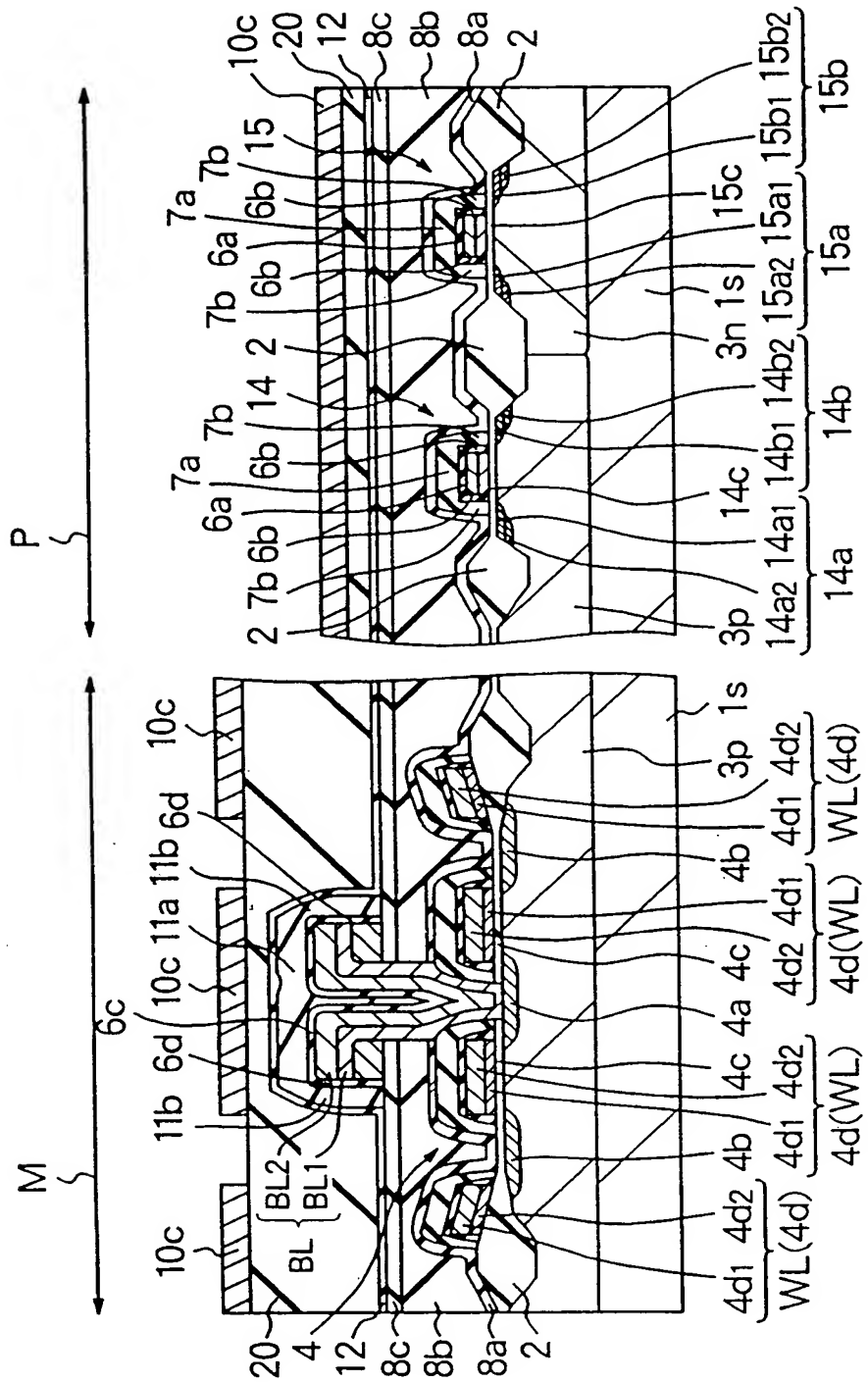


FIG. 9b

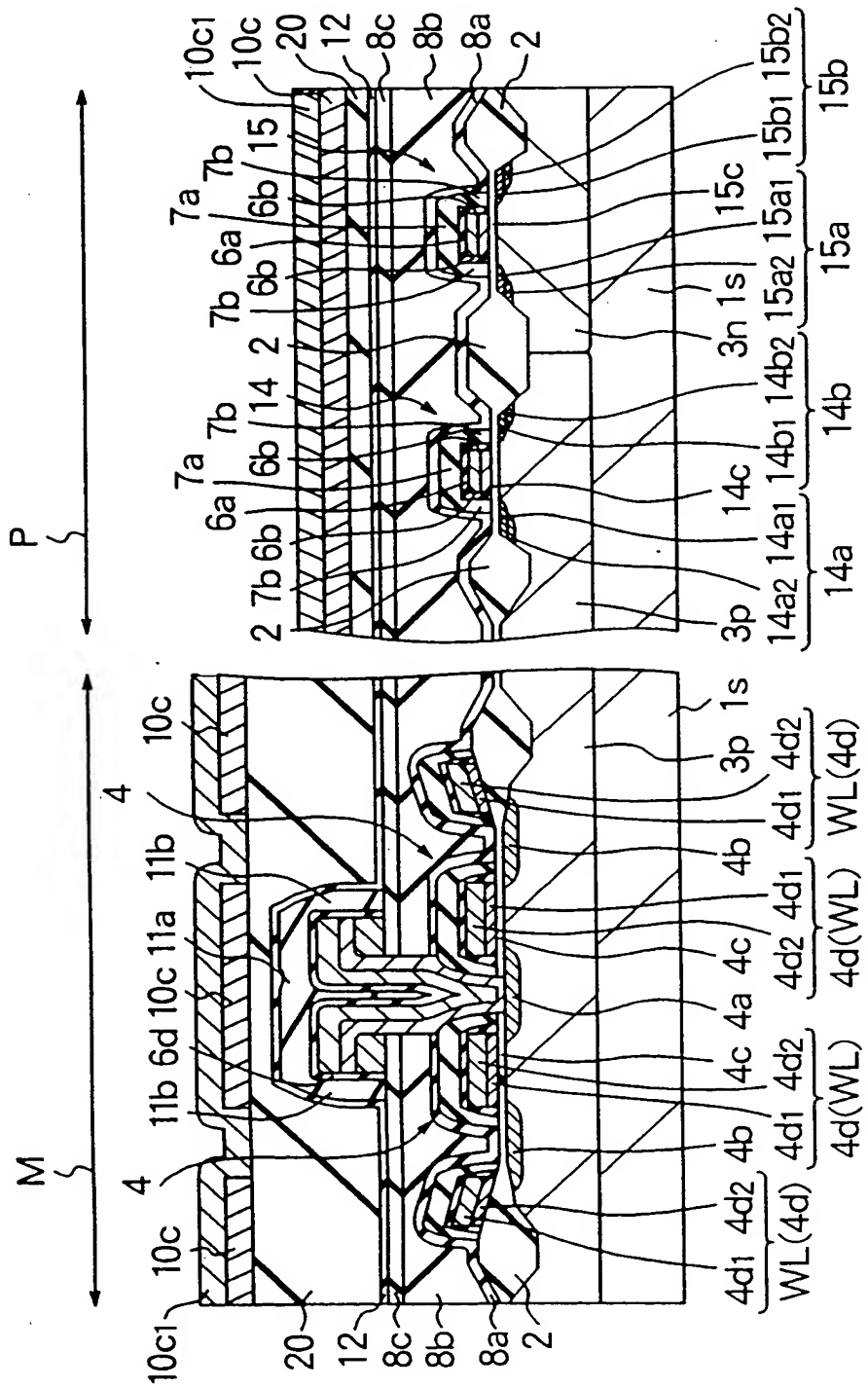


FIG. 9c

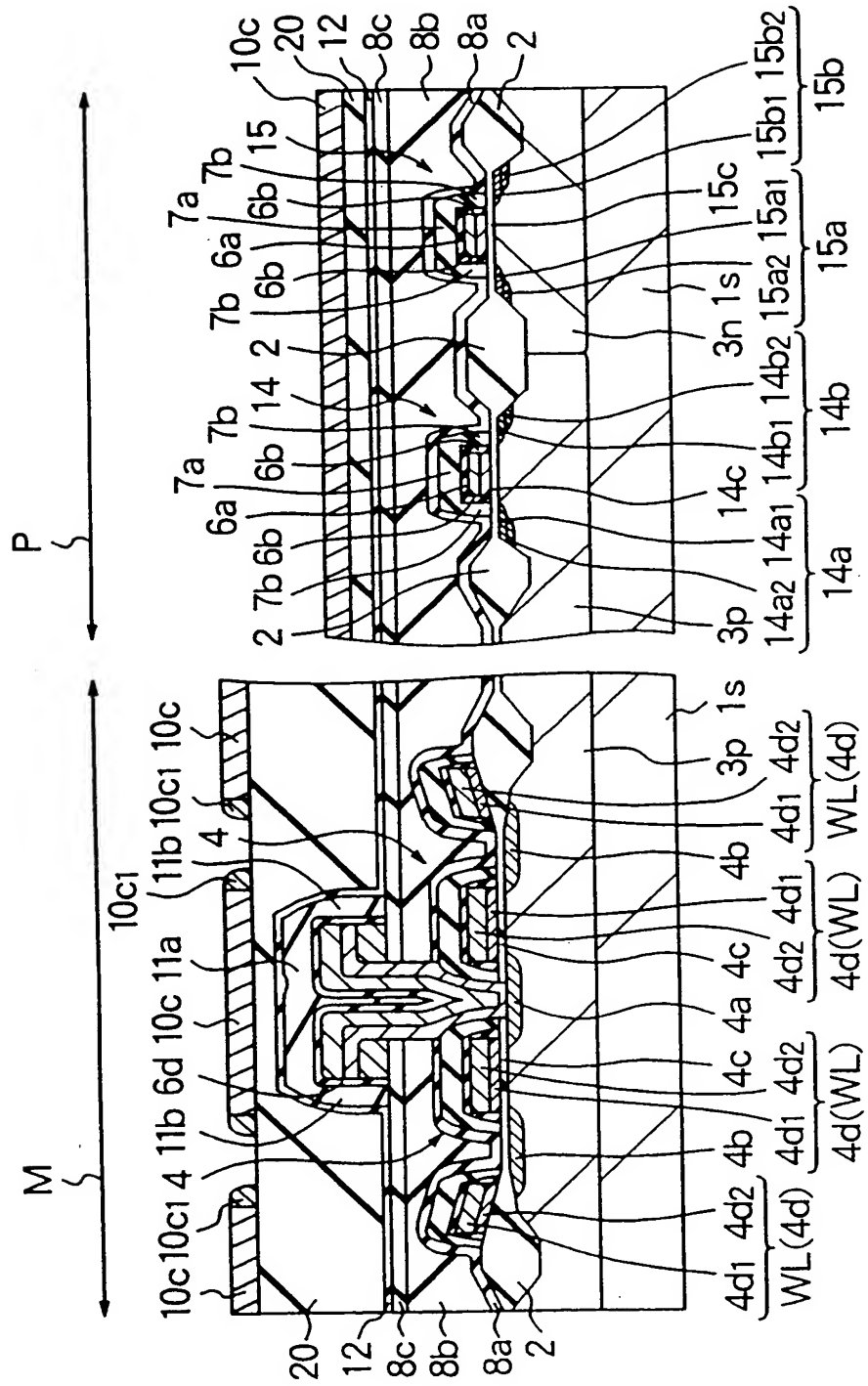
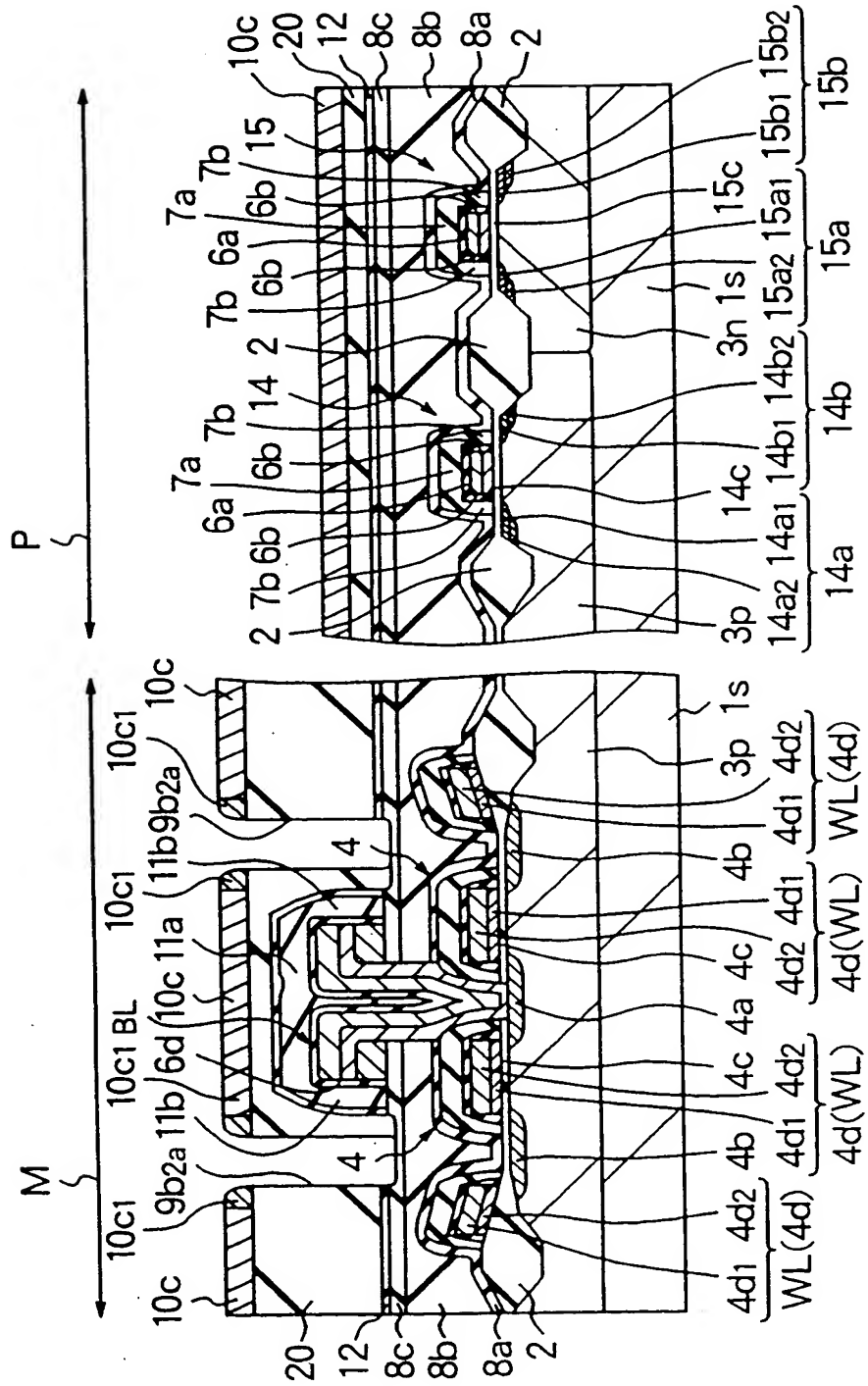
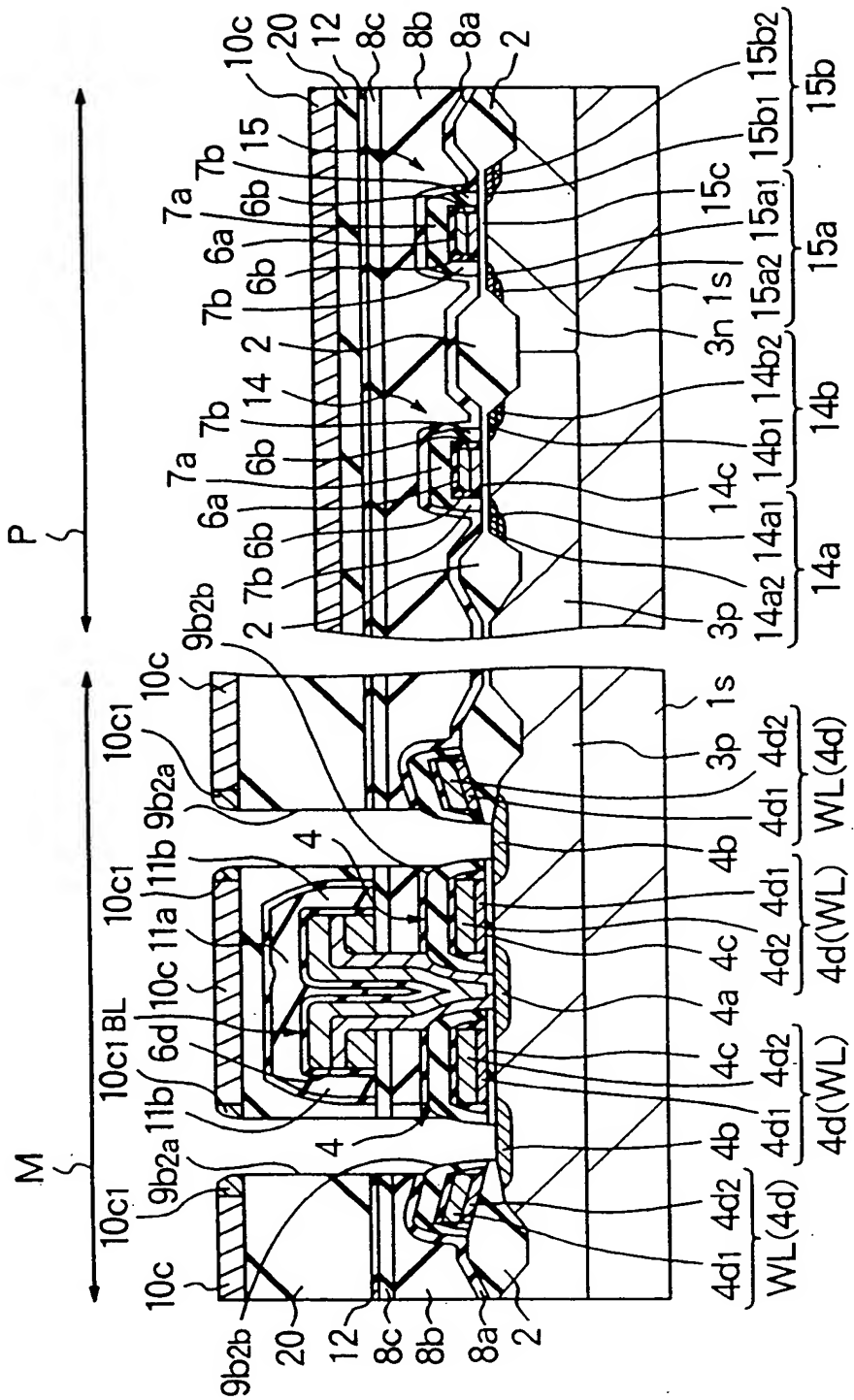


FIG. 9d





[illegible]